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Paper 155
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

RICHARD E. PEREGO, STEFANOS SIDIROPOULOS
and ELY TSERN
Junior Party
(Patent 6,502,161)

v.

ROBERT ALLEN DREHMEL, KENT HAROLD HASELHORST,
RUSSELL DEAN HOOVER and JAMES ANTHONY MARCELLA
Senior Party
(Application 11/203,652)

Patent Interference No. 105,467 (JL)
(Technology Center 2100)

Before: RICHARD E. SCHAFER, JAMESON LEE, and RICHARD TORCZON, *Administrative Patent Judges*.

LEE, *Administrative Patent Judge*.

DECISION ON PRIORITY

A. Introduction

The interference is before a merits panel of the Board for a decision on the question of priority. Both parties filed a motion for priority of invention -- Perego's Motion 9 and Drehmel's Motion 1. Drehmel has also filed Miscellaneous Motion 2 to exclude a multitude of Perego exhibits.

B. General findings of fact

The junior party is named inventors Richard E. Perego, Stefanos Sidiropoulos, and Ely Tsern (collectively "Perego") and the real party in interest is Rambus, Inc. ("Rambus"). Paper 4.

Junior party Perego is involved on the basis of Patent 6,502,161, based on Application 09/479,375, filed January 5, 2000.

The senior party is named inventors Robert Allen Drehmel, Kent Harold Haselhorst, Russell Dean Hoover, and James Anthony Marcella (collectively "Drehmel") and the real party in interest is IBM Corporation ("IBM"). Paper 9.

Senior party Drehmel is involved on the basis of Application 11/203,652, filed August 15, 2005.

Rambus presented claims and sought an interference with IBM.

This interference was declared on August 15, 2006. Paper 1.

At the time of declaration of interference, Drehmel was accorded benefit of Application 10/747,820, filed December 30, 2003, and Application 09/439,068, filed November 12, 1999. Application 09/439,068 is now issued as Patent 6,526,469.

The sole count is Count 1, which reads (Paper 1, p. 4):

Perego 6,502,161 claim 1

or

Drehmel 11/203,652 claim 11

Drehmel's claim 11 is copied from Perego's claim 1 and the two claims are identically worded.

The claims of the parties are as follows:

Perego Patent 6,502,161	1-49
Drehmel Application 11/203,652	11-59

The claims of the parties which have been designated as corresponding to Count 1 and therefore are involved (35 U.S.C. § 135(a) in the interference) are:

Perego Patent 6,502,161	1-49
Drehmel Application 11/203,652	11-59

The claims of the parties which have been designated as *not* corresponding to Count 1 and therefore are not involved in the interference are:

Perego Patent 6,502,161	None
Drehmel Application 11/203,652	None

Perego's claim 1 reads as follows:

1. A memory system comprising:

a memory controller having an interface that includes a plurality of memory subsystem ports;

a first memory subsystem including:

a buffer device having a first port and a second port, and

a plurality of memory devices coupled to the buffer device via the second port, wherein data is transferred between at least one memory device of the plurality of memory devices and the memory controller via the buffer device; and

a plurality of point-to-point links, each point-to-point link of the plurality of point-to-point links having a connection to a respective memory subsystem port of the plurality of memory subsystem ports, the plurality of point-to-point links including a first point-to-point link to connect the first port to a first memory subsystem port of the plurality of memory subsystem ports.

C. The invention

The invention of Count 1 is readily understood by reference to Fig. 3A of Perego's U.S. Patent 6,502,161 (Ex. 2001).

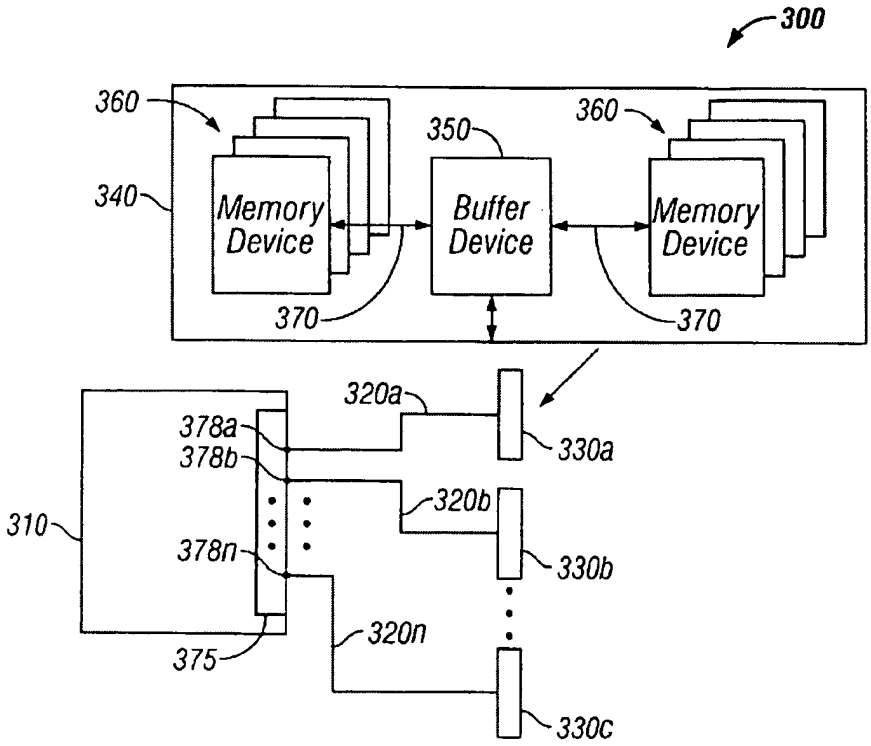


FIG. 3A

Perego's Patent Fig. 3A depicts a memory system.

With respect to Figure 3A, the disclosed Perego invention is directed to a memory system architecture which includes a memory controller communicating to at least one memory subsystem, *e.g.*, a buffered memory module. (Ex. 2001 3:48-51). An independent point-to-point link is used between the controller and each memory subsystem to eliminate physical inter-dependence between memory subsystems. (Ex. 2001 3:51-54).

Memory subsystem 300 includes a controller 310, a plurality of point-to-point links 320a-320n, and a plurality of memory subsystems 330a-330n. (Ex. 2001 5:49-52). A more detailed embodiment of memory subsystem 330a is illustrated as element 340 also in Figure 3A. Buffer device 350 and a plurality of memory devices 360 are disposed on memory subsystem 340.

(Ex. 2001 5:54-55). An interface 375 is disposed on controller 310 and it includes a plurality of memory subsystem ports 378a-378n. (Ex. 2001 5:57-58). A memory subsystem port sends and receives sends and receives data, addressing and controlling information, over one of the point-to-point links 320a-320n. (Ex. 2001 5:60-63).

A major contrast with the prior art lies in the difference between the use of individual point-to-point links in Perego's invention to connect the memory controller and each memory subsystems on the one hand, and the use of a common bus line to do the same on the other. Figure 1 of Perego's Patent 6,502,161, is reproduced below, illustrating prior art using a common bus line:

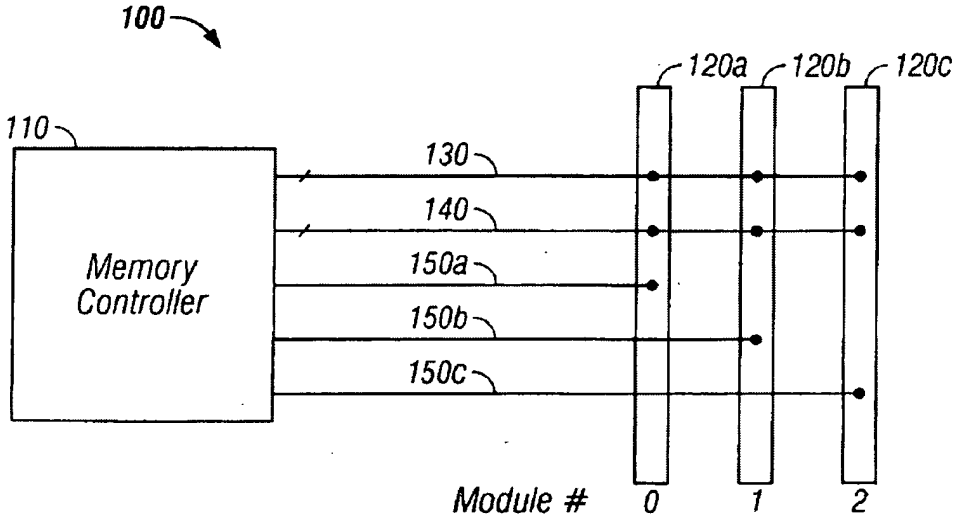


FIG. 1
(Prior Art)

Perego's Patent Fig. 1 depicts a memory system.

In the prior art system shown above, the address lines and control signals of control/address bus 130 are bussed and "shared" between each of modules 120a-120c to provide row/column addressing and read/write,

precharge, refresh commands, etc., to memory devices on a selected one of modules 120a-120c. (Ex. 2001 1:35-39).

Figure 2A of Perego's Patent 6,502,161, is reproduced below, illustrating a more improved prior art using a common bus 260 with shortened stub lines connecting to each module (Ex. 2001 2:31-40):

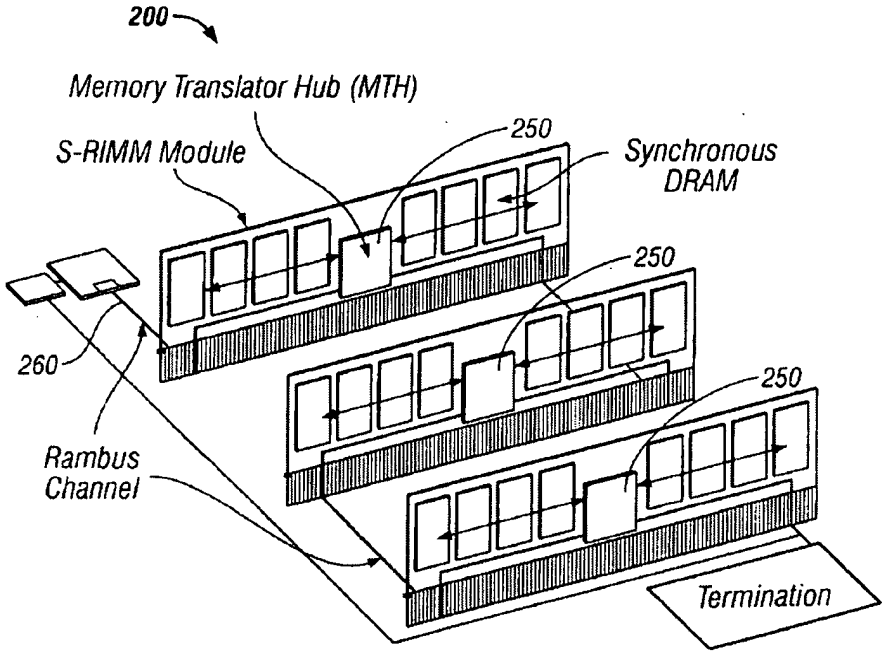


FIG. 2A
(Prior Art)

Perego's Patent Figure 2A depicts a memory system

The common bus line or Rambus Channel 260 connects to each memory module through respective short stub lines which tap into the common bus line at a corresponding Memory Translator Hub (MTH) serving as a connection point between the memory module and the bus. (Ex. 2001 2:34-40).

Detailed internal connections at each MTH are not illustrated. Although the S-RIMM memory modules appear serially connected rather

than connected in parallel, in fact they are still connected in parallel to the common bus line 260 through the MTHs.

A serial connection contradicts the description of line 260 as a common bus with a termination point beyond the last connected module.

In Figure 2A of Perego's involved patent, the common bus line or Rambus Channel is arranged in a visually snakelike or serpentine daisy chain configuration which winds its way from one MTH hub to the next, switching entry and exit direction at each subsequent MTH. The snakelike daisychain connects to each module through a respective MTH.

As is explained in the Perego specification (Ex. 2001 2:45-48), in the bussed approach of Figure 2A, the signal lines also become loaded with a load capacitance associated with each bus connection point, and the load capacitances connected to multiple points along the length of the signal line may degrade signaling performance. (Ex. 2001 2:56-58).

As shown in Perego's Figure 3A, in Perego's disclosed invention separate and independent point-to-point links 320a-320n are used to connect the memory controller 310 to the buffer device 350 of each memory module 330a-330c (element 340 is an expanded view of a memory module):

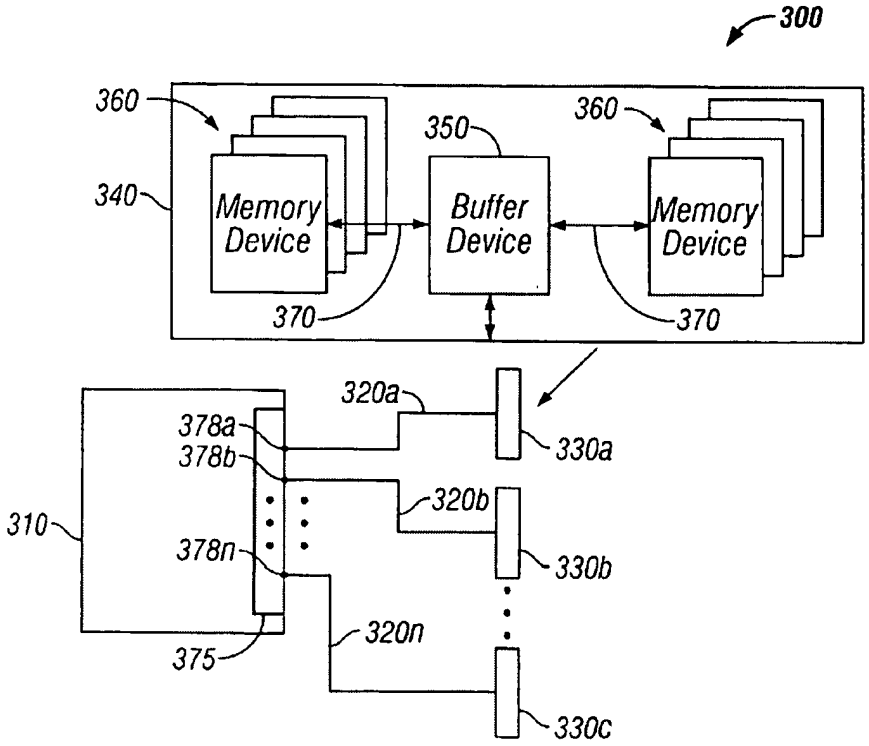


FIG. 3A

Perego's Patent Figure 3A depicts a memory system

The term "point-to-point link" is expressly defined in Perego's specification as follows (Ex. 2001 7:39-43):

> The term "point-to-point link" denotes one or a plurality of signal lines, each signal line having only two transceiver connection points, each transceiver connection point coupled to transmitter circuitry, receiver circuitry or transceiver circuitry.

Perego's Figure 3B discloses an alternative invention, one in which the point-to-point links do not connect the common memory controller 310 directly to the buffer device 350 in individual memory modules 330a-330c, but to a connector 380a-380n which is in turn connected to a corresponding matching connector 390a-390c on the memory module. And then the buffer device in the memory module is connected through another link to the

connector 390a-390c (The reference 370a in Figure 3B is believed to be intended as 390a). Perego's Figure 3B is reproduced below:

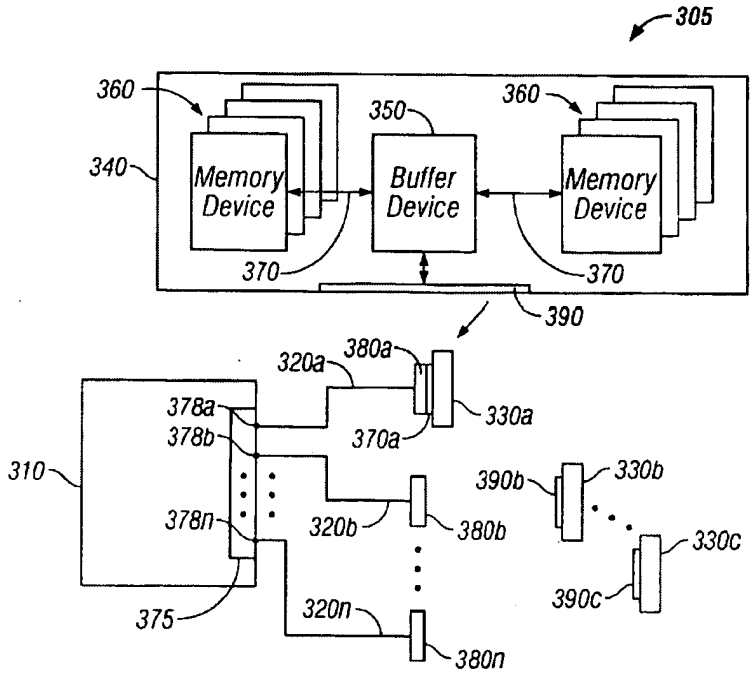


FIG. 3B

Perego's Patent Figure 3B depicts a memory system

With respect to the alternative invention of Figure 3B, Perego's specification states (Ex. 2001 6:14-24):

> Corresponding mating connectors 380a-380n are connected to a connection point of each point-to-point link 320a-320n. Each of mating connectors 380a-380n interface with connectors 390a-390c to allow removal/inclusion of memory subsystems 330a-330c in memory system 305. In one embodiment, mating connectors 380a-380n are sockets and connectors 390a-390c are edge connectors disposed on an edge of each substrate 330a-330c. Mating connectors 380a-380n, are attached to a common substrate shared with point-to-point connections 320a-320n and controller 310.

Perego's specification expressly limits the number of transceiver connection points on a point-to-point link to only two. (Ex. 2001 7:39-43).

Perego's Figure 3B illustrates point-to-point links 320a-320n each of which connects memory controller 310 to a connector 380a-380n. The connector is not a transmitter, receiver, or transceiver, but each point-to-point link has two transceiver connection points.

One end point of each point-to-point link is coupled to the memory controller 310. The other end point of the same link is coupled to a connector 380a-380n which is coupled to memory controller 310 by the link itself. A transceiver connection point does not require a direct connection to a transmitter, receiver, or transceiver.

As shown in Figure 3B, on each point-to-point link 320a-320n, the connection point at each connector 380a-380n is a transceiver connection point, constituting the second transceiver connection point for the point-to-point link 320a-320n. An annotated copy of Figure 3B is reproduced below, with added red arrows pointing to the two transceiver connection points of each point-to-point link 320a-320n:

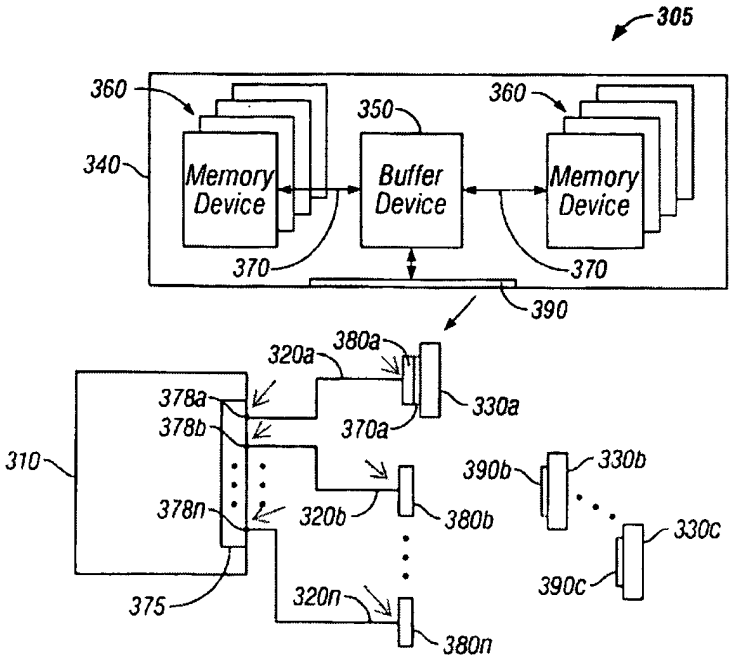


FIG. 3B

Perego's Patent Figure 3B depicts a memory system

Each connection from memory controller 310 to a buffer device 350 in a memory module 330 (illustrated in more detail as element 340) includes more than two transceiver connection points, the two shown above in red for each point-to-point link 320a-320n, one at the immediate and final connection to the buffer device 350 itself, one at the interface connector 390 to which the buffer device 350 is connected, and one at the junction between connectors 390 and 380.

Together there are five transceiver connection points between the memory controller and each buffer device 350. At the very least, there are three transceiver connection points even if reference numeral 390 does not identify a separate connector.

As shown in Figure 3B, the link from memory controller 310 all the way to a buffer device 350 is not a point-to-point link which by definition

can have no more than two transceiver connection points. Perego's specification also does not describe that connection as a point-to-point link.

D. Priority dates alleged in motions

In its priority motion before us, Perego contends that it has established the following dates of conception of the invention of Count 1.

Event	Perego
Conception	14 May 1999
Conception	15 June 1999
Conception	25 June 1999

To prevail in its priority motion, Perego must establish one of the three alleged conception of invention dates together with reasonable diligence in reducing the conceived invention to practice from a time just prior to Drehmel's entry into the field (a date yet to be determined) until January 5, 2000, the time of filing of Perego's involved Patent 6,502,161.

E. Principles of law

Conception is the formation "in the mind of the inventor of a definite and permanent idea of the complete and operative invention, as it is therefore to be applied in practice." *Coleman v. Dines*, 754 F.2d 353, 359 (Fed. Cir. 1985). Proof of conception must demonstrate possession of every single feature of the count. *Davis v. Reddy*, 620 F.2d 885, 889 (CCPA 1980).

Conception also must be proved by corroborating evidence which shows that the inventor disclosed to others his complete thought expressed in such clear terms as to enable those skilled in the art to make the invention.

Coleman, 754 F.2d at 359. However, there is no final single formula that must be followed in proving corroboration. *Berry v. Webb*, 412 F.2d 261, 266 (CCPA 1969). Rather, the sufficiency of corroborative evidence is determined by a "rule of reason." *Price v. Symsek*, 988 F.2d 1187, 1195 (Fed. Cir. 1993); *Berry*, 412 F.2d at 266.

A deciding tribunal must make a reasonable analysis of all of the pertinent evidence to determine whether the inventor's testimony is credible. *Price*, 988 F.2d at 1195. The purpose of requiring corroboration is to prevent fraud by providing independent confirmation of the inventor's testimony. *See Berry*, 412 F.2d at 266; *Reese v. Hurst*, 661 F.2d 1222, 1225 (CCPA 1981) ("[E]vidence of corroboration must not depend solely on the inventor himself.").

F. Perego's alleged conception of 14 May 1999

Findings of fact

The named inventors of Perego's involved Patent 6,502,161, are Richard E. Perego, Stefanos Sidiropoulos, and Ely Tsern.

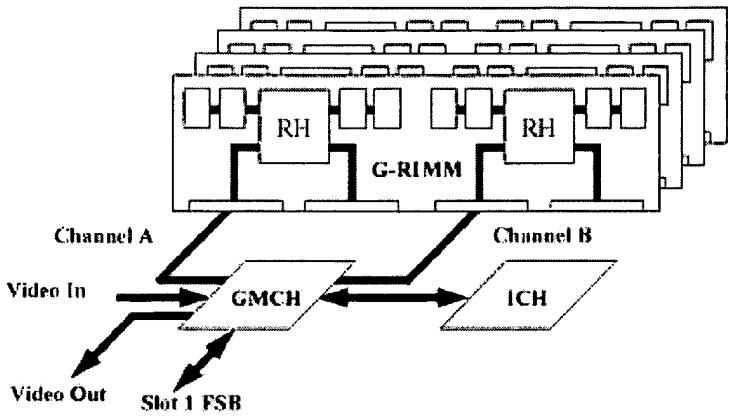
Upon joining Rambus on April 1, 1999, Mr. Perego was assigned to the Logical Architecture Group managed by Dr. Ely Tsern. (Ex. 2143 ¶¶ 1-3, 6; Ex. 2144 ¶¶ 1, 5; Ex. 2145 ¶ 5).

By at least May 14, 1999, Mr. Perego wrote a technical specification titled "3D Parallel Rendering Architecture Proposal" which is Exhibit 2059 in this interference. (Ex. 2143 ¶ 11; Ex. 2144 ¶ 10; Ex. 2145 ¶ 9; Ex. 2148 ¶ 4). Hereinafter, we will refer to that document (Ex. 2059) as "the May 14th Parallel Rendering Proposal."

Figure 3-1 of the May 14th Parallel Rendering Proposal is reproduced below, together with the sentence introducing the figure and the associated listing of the applicable nomenclature:

The diagram below illustrates the basic proposal for mainstream systems.

Figure 3-1: Graphics RIMM Based UMA System Proposal



The diagram above uses Intel's latest hub-centric nomenclature:

GMCH = Graphics and Memory Controller Hub

ICH = IO Controller Hub

RH = Rendering Hub

Figure 3-1 discloses a memory system including a memory controller GMCH. The GMCH is connected by two channels A and B to a first memory module G-RIMM. Configured on the first memory module are two Rendering Hubs (RH) (Ex. 2059 3-13:2-3). Each Rendering Hub RH serves as a buffer to which a separate plurality of memory units are connected. Behind the first memory module are a plurality of additional memory modules of like configuration. The multiple memory modules are described in the written portion of the May 14th Parallel Rendering Proposal as connected to each other via either an inline bus or a snakelike daisy chain

(Ex. 2059 3-13:7-8). The embodiment illustrated in Figure 3-1 has the "snakelike daisy chain" configuration (Ex. 2059 3-13:7-10).

A "snakelike daisy chain" configuration is one depicting a serial connection. According to Computer Dictionary, Second Edition, Microsoft Press (1994), the term "daisy chain" refers to: "[a] set of devices connected in a series." The definition is sufficiently broad to cover a configuration that merely appears to depict a serial connection but is in fact an inline bus which connects to multiple elements in parallel.

As is discussed above, the prior art system shown in Figure 2A of Perego's involved patent illustrates a plurality of memory modules (S-RIMM) which are actually connected in parallel to the Rambus channel 260 but in a serpentine winding configuration that illustrates a snakelike daisy chain of modules seemingly connected in series because of short stub lines.

Each communication link in a serial connection need not be free of other system components or intermediate connectors. For instance, as is illustrated in Figure 3-1 of the May 14th Parallel Rendering Proposal, the communication link from the memory controller GMCH to one buffer device RH via Channel A is broken up into two segments joined by a connector at an interface to the memory module. Likewise, the communication link from the memory controller GMCH to the other buffer device RH via Channel B is also broken up into two segments joined by a connector at another interface to the memory module.

Channel A connects to the memory controller GMCH and Channel B separately connects to the memory controller GMCH. (Ex. 2059 Fig. 3-1). Channel A connects to a connector, shown as a rectangular element on the perimeter of memory module G-RIMM. Channel B connects to a separate

connector, also shown as a rectangular element on the perimeter of memory module G-RIMM. (Ex. 2059 Fig. 3-1).

A first buffer device (RH) on the left side of memory module G-RIMM is connected through a first port of its own to the port or connector on the G-RIMM to which Channel A is connected, and a second buffer device (RH) on the right side memory module G-RIMM is connected through a first port of its own to the port or connector on the G-RIMM to which Channel B is connected. (Ex. 2059 Fig. 3-1). The communication link between memory controller GMCH and the first buffer device and the communication link between memory controller GMCH and the second buffer device do not overlap. Each buffer device RH on memory module G-RIMM, through a second port of its own, connects to a plurality of memory units. (Ex. 2059 Fig. 3-1).

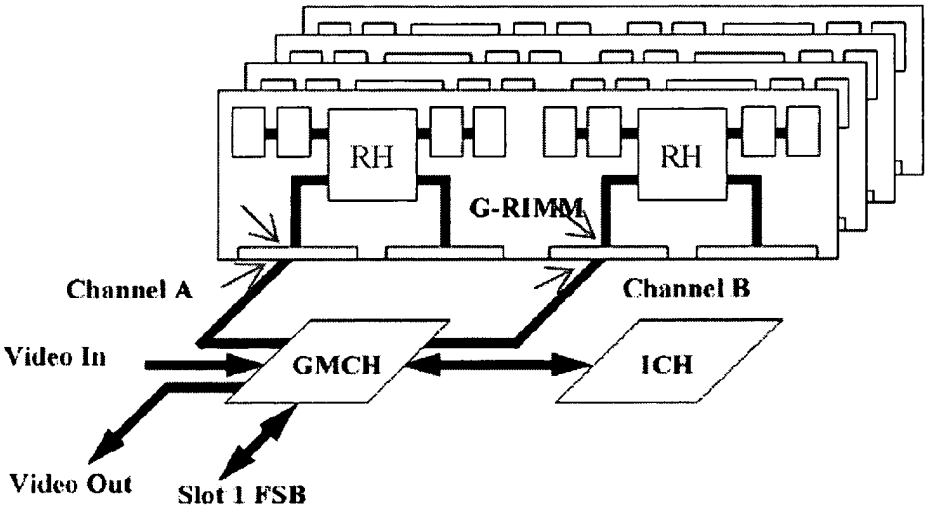
The communication link from memory controller GMCH to the first port of the buffer device RH on the left side of memory module G-RIMM is not a point-to-point link. The two points of connection to the intermediate connector are two additional transceiver connection points on the communication link other than the two end points.

The communication link from memory controller GMCH to the first port of the buffer device RH on the right side of memory module G-RIMM is not a point-to-point link. The two points of connection to the intermediate connector are two additional transceiver connection points on the communication link other than the two end points.

As shown in Figure 3-1 of the May 14th Parallel Rendering Proposal, each communication link from the memory controller GMCH to a buffer device RH ("Rambus Hub") includes two segments, a first segment

extending from the memory controller GMCH to a connector on a memory module including the buffer device, and a second segment from that connector to the buffer device. An annotated copy of Figure 3-1 is reproduced below, with added red arrows pointing to where the first and second segments of the communication link connect to an intermediate connector:

Figure 3-1: Graphics RIMM Based UMA System Proposal



As illustrated in the May 14th Parallel Rendering Proposal, each communication link between the memory controller GMCH and a buffer device RH includes four transceiver connection points, with each transceiver connection point coupled to transmitter circuitry, receiver circuitry, or transceiver circuitry.

The intermediate connector is not a transmitter, receiver, or a transceiver circuitry. But each point of connection identified by a red arrow in the annotated Figure 3-1 of the May 14th Parallel Rendering Proposal

above is coupled by a communication link segment to either the memory controller GMCH or a buffer device RH which is transceiver circuitry.

On Page 3-19 of the May 14th Parallel Rendering Proposal, in the section listing the advantages of the design, lines 27-33 state the following:

> For large capacity designs (8 to 16 DRAMs per G-RIMM), it is possible to reduce the pin count and associated cost of the DRAMs by using a narrower device width (x4, for example) and accessing all devices in parallel, while preserving bandwidth. This potentially enables point-to-point, unidirectional, differential signalling, which could increase bandwidth further. Write buffering in RH could allow a narrower, unidirectional write data bus (x2 for example) if an appropriate stall mechanism is devised.

The "point-to-point" signalling referred to in the above-quoted discussion is directed to communication in each memory module G-RIMM to DRAM memory devices shown in Figure 3-1 as small rectangles in each G-RIMM, and not communication from a memory controller GMCH to a plurality of G-RIMMs through a buffer in each G-RIMM.

Analysis

For its priority motion, party Perego bears the burden of proof to establish that it is entitled to the relief requested. 37 C.F.R. § 41.121(b).

Conception is the formation in the mind of the inventor of a definite and permanent idea of the complete and operative invention, as it is therefore to be applied in practice, *Coleman v. Dines*, 754 F.2d at 359, and proof of conception must demonstrate possession of every single feature of the count. *Id.*; *Davis v. Reddy*, 620 F.2d at 889. Every limitation of the count must have been known to the inventor at the time of the alleged conception. *Coleman v. Dines*, 754 F.2d at 359.

A particular feature of the count is:

> a plurality of point-to-point links, each point-to-point link of the plurality of point-to-point links having a connection to a respective memory subsystem port of the plurality of memory subsystem ports, the plurality of point-to-point links including a first point-to-point link to connect the first port to a first memory subsystem port of the plurality of memory subsystem ports.

In his declaration testimony (Ex. 2143 ¶ 19), inventor Richard E. Perego refers to the May 14th Parallel Rendering Proposal, in particular Figure 3-1, which has been reproduced above. Also citing page 19 of the May 14th Parallel Rendering Proposal, and without meaningful explanation, the testimony in the same paragraph further states that as disclosed, "the channels" (Channels A and B in Figure 3-1) could be point-to-point and allow for unidirectional, and differential signalling, which could increase bandwidth. For reasons discussed below, we do not credit that testimony of Richard Perego. Nothing in the law requires the fact finder to credit the unsupported assertions of a witness. *See Rohm and Haas Co. v. Brotech Corp.*, 127 F.3d 1089, 1092 (Fed. Cir. 1997).

The pertinent description on page 19 of the May 14th Parallel Rendering Proposal is that appearing on lines 27-33. The entire paragraph has been reproduced above. As is determined in our finding above, the description is directed to signalling in each memory module G-RIMM to a plurality of DRAM memory devices shown in Figure 3-1 as small rectangles in each G-RIMM, and not communication from a memory controller GMCH to a plurality of G-RIMMs through a buffer in each G-RIMM. Channels A and B connecting memory controller GMCH to a memory module G-RIMM

are plainly not the subject of that discussion, and Perego's declaration does not explain why Channels A and B are what is discussed. Perego who has the burden of proof has not established that the passage actually refers to communication between controller GMCH and the G-RIMM modules.

Paragraph 17 of the supporting declaration of Dr. Steven Woo (Ex. 2145), the Technical Director of Rambus, Inc., embodies the same deficiencies as noted above with regard to the declaration of Richard Perego in connection with the point-to-point link requirement for the link between the memory controller GMCH and the buffer in memory module G-RIMM. He does not explain why the passage in lines 27-33 on page 3-19 of the May 14th Parallel Rendering Proposal, which on its face concerns communication within the G-RIMM module to and from the plurality of DRAMs, describes the external link from controller GMCH to buffer RH of each G-RIMM. Accordingly, we also do not credit his testimony that the May 14th Parallel Rendering Proposal describes the point-to-point link feature of the count.

Co-inventor Dr. Ely Tsern testified that he recalls seeing Richard Perego's Parallel Rendering Proposal (Exhibit 2059) or a document containing substantially the same information on or about May 13, 1999. (Ex. 2144 ¶ 10). Citing to page 3-19 of the Parallel Rendering Proposal, Dr. Tsern, like Dr. Steven Woo and Richard Perego himself, states that Richard Perego "discloses that Channels A and B may be point-to-point links." (Ex. 2144 ¶ 10). As is already discussed above in connection with Dr. Woo and Richard Perego's testimony, Dr. Tsern's testimony concerning Channels A and B in the Parallel Rendering Proposal being described in that proposal as possibly point-to-point links lacks reasonable support and thus is also not credited with persuasive weight. Nothing on page 3-19 of the proposal

describes that either Channel A or Channel B in Figure 3-1 of the Parallel Rendering Proposal may be a point-to-point link. Dr. Tsern also does not point to any particular part of that page of the proposal. And Dr. Ely Tsern is himself a co-inventor and cannot provide the necessary independent corroboration for an inventive fact. *See Brown v. Barbacid*, 276 F.3d 1327, 1335 (Fed. Cir. 2002).

That the signaling between the buffer RH in each G-RIMM module and the plurality of DRAMs in the G-RIMM module may be through point-to-point links does not mean the connection from memory controller GMCH to buffer RH in each G-RIMM module has to be through a point-to-point link. Even assuming that the former would have rendered obvious the latter, it does not establish conception by junior party's inventors of the feature of using a plurality of point-to-point links which connect to a respective port on the memory controller, including one which connects to the buffer. The test for conception is not obviousness. Perego must demonstrate possession of every single feature of the count. *Davis v. Reddy*, 620 F.2d at 889.

In any event, and adding to the deficiency of Perego's motion, it is noted that the term "point-to-point link" has a special definition in the specification of Perego's involved patent. (Ex. 2001 7:39-43). Perego has not demonstrated that that special definition is the same as the ordinary meaning of that term in the art of the invention of the count. Thus, on this record it is not even clear whether "point-to-point link" means the same in Perego's specification and in the May 14th Parallel Rendering Proposal.

We have also determined in the findings above that as illustrated in Figure 3-1 of the May 14th Parallel Rendering Proposal, the Channel A link in the portion between memory controller GMCH and buffer RH has four

transceiver connection points, and the Channel B link in the portion between memory controller GMCH and buffer RH also has four transceiver connection points. As is defined in the specification of Perego's patent, however, a point-to-point link can have no more than two transceiver connection points. (Ex. 2001 7:39-43). Thus, the portion of Channels A and B shown in Figure 3-1 of the May 14th Parallel Rendering Proposal between memory controller GMCH and buffers RH are not point-to-point links.

In addition, each of Channels A and B does not simply terminate at the buffer RH of the first memory module G-RIMM. It winds its way through each successive memory module G-RIMM in a snakelike daisy chain configuration. The segment between memory controller GMCH and the buffer RH of the first G-RIMM is just one portion of the entire channel, and extends continuously to the next segment connecting to the G-RIMM next in line in the daisy chain. Consequently, there are even more transceiver connection points on the same channel and coupled to the segment between memory controller GMCH and the first G-RIMM module, further disqualifying that segment as a point-to-point link.

Perego's motion further refers to an electronic mail message dated May 13, 1999, from Mr. Sheffler (Ex. 2058), which states "Using buffers/repeaters on a module (as described by Rich) is one possibility." That expression does not indicate the use of a point-to-point link from any component to any other component.

In Paragraph 19 of inventor Richard E. Perego's declaration, he notes that in the May 14th Parallel Rendering Proposal he described that the memory controller and the memory modules may be connected by way of a "snakelike daisy chain." The daisy chain configuration is described on page

3-13 as being "illustrated below," *i.e.*, Figure 3-1. Richard E. Perego further states in the same declaration paragraph that in a "snakelike daisy chain," the memory controller is connected to the rendering engine of the first memory module by a point-to-point link, and that subsequent memory modules are connected via a separate and isolated set of point-to-point links. Mr. Perego cites page 18 of the May 14th Parallel Rendering proposal, but nothing on the cited page supports the assertion.

Moreover, as we have already explained in detail above in connection with the daisy chain configuration illustrated in Figure 3-1, the link from memory controller GMCH to the rendering engine, a buffer, of the first memory module G-RIMM, is not a point-to-point link based on the definition of "point-to-point link" given in Perego's specification. There are at least four transceiver connection points on that first link, and subsequent links are all segments of the same Channel A or Channel B which connects all of the modules G-RIMM. Each of the segments is connected to all of the transceiver connection points located on the same channel.

Note also that if indeed there are separate and isolated segments connecting each successive module, there would have to be circuitry in each G-RIMM module designed for handling information that is received but intended for another module. No such circuitry is described as present within any G-RIMM module. The evidence does not support the assertion that the memory controller GMCH is connected to a first G-RIMM module by a point-to-point link, or that subsequent successive pairs of G-RIMM modules are each connected by a separate and isolated point-to-point link.

Mr. Perego's assertion is contrary to the disclosure of the May 14th Parallel Rendering Proposal itself. We credit the disclosure of the May 14th

Parallel Rendering Proposal more than the unsupported characterization of Richard E. Perego. We note also the prior art illustrated in Figure 2A of Perego's involved patent. It is in a "snakelike daisy chain" configuration and yet described in Perego's involved patent as employing a common channel or bus 260. (Ex. 2001 2:34-48). A common bus that connects all of the G-RIMM modules is neither a point-to-point link nor a plurality of point-to-point links. We are unpersuaded by Richard E. Perego's testimony that the May 14th Parallel Rendering Proposal describes a point-to-point link connecting memory controller GMCH to a buffer of a G-RIMM module.

G. Perego's alleged conception of 15 June 1999

In the alternative, Perego alleges conception of the subject matter of the count by June 15, 1999. Perego relies on all of the evidence discussed above in connection with the alleged conception by May 14, 1999, and additional evidence. In particular, Perego relies on another document said to have been generated by Richard E. Perego and shared with his colleagues by June 15, 1999, which is said to be a slightly modified version of the May 14th Parallel Rendering Proposal. Hereinafter, the document is referred to as "Parallel Rendering Proposal 2" and it is Exhibit 2063 in the record.

Drs. Woo and Tsern testified that they received Parallel Rendering Proposal 2 from Richard E. Perego on June 15, 1999. (Ex. 2145 ¶ 18; Ex. 2144 ¶ 11). Perego represents (Motion 12:19-22) that Parallel Rendering proposal 2 and the May 14th Parallel Rendering proposal "are substantially the same, and do not differ in any relevant respect." Accordingly, we assume that the two documents have the same content and the findings we have made above with respect to the May 14th Parallel Rendering proposal are equally applicable to Parallel Rendering Proposal 2.

For the same reasons as explained above on why Perego has failed to demonstrate conception of the subject matter of the count by May 14, 1999, Perego has also failed to demonstrate conception of the subject matter of the count by June 15, 1999.

H. Perego's alleged conception of 25 June 1999

In the alternative, Perego alleges conception of the subject matter of the count by June 25, 1999. Perego relies on all of the evidence discussed above in connection with the alleged conception by June 15, 1999, and additional evidence. In particular, Perego relies on another document said to have been generated by Richard E. Perego by June 25, 1999, which is said to be a revised version of the May 14th Parallel Rendering Proposal and Parallel Rendering Proposal 2. Hereinafter, the document is referred to as "Parallel Rendering Proposal 3" and it is Exhibit 2065 in the record.

Perego represents (Motion 14:3-4) that Parallel Rendering Proposal 3 is substantially the same as Parallel Rendering Proposal 2 and the May 14th Parallel Rendering Proposal. Also, Perego asserts (Motion 14:5-6) that Parallel Rendering Proposal 3 satisfies the subject matter of the count for similar reasons as Parallel Rendering Proposal 2 and the May 14th Parallel Rendering Proposal. Accordingly, we assume that the documents have the same substantive content and the findings and conclusions we have made above with respect to the May 14th Parallel Rendering proposal are equally applicable to Parallel Rendering Proposal 3.

In ¶ 22 of Richard E. Perego's declaration (Ex. 2143), it is noted that page 9 of Parallel Rendering Proposal 3 states: "High-bandwidth memory access for Rendering Engine(s) - generally allows point-to-point connections which allow higher interface frequency." The same disclosure is noted by

Dr. Steven Woo in ¶ 19 of his declaration. (Ex. 2145). As is the case with cited portions on page 3-19 of the May 14th Parallel Rendering Proposal already discussed, however, the cited text refers to communication between the Rendering Engines and the plurality of memory units (RAMs) all contained within each G-RIMM module, and not to connections between the external memory controller GMCH and each Rendering Engine. Perego has not explained why the converse is true, *i.e.*, why the reference to point-to-point connections refers to links between the memory controller and each G-RIMM module rather than the links between the Rendering Engine and each random access memory RAM.

Dr. Tsern testified that on June 17, 1999, he received an email (Ex. 2064) from Richard Perego, which email noted an idea involving buffered solutions with point-to-point differential links. (Ex. 2144, ¶ 11). But the email does not identify or explain the point-to-point links as existing between the memory controller and each buffer, and not between each buffer and the memory RAM units connected to each buffer. It is not enough to show conception that point-to-point links are used somewhere.

Also, Dr. Tsern further testified that he "would have understood" the idea in Richard Perego's email as referring to Richard Perego's "buffered module concept that is the subject matter of the count" (Ex. 2144, ¶ 11). He does not state that he actually "understood" the matter as such, but "would have understood" as in a speculation. And that does not matter, because Perego has not established that there ever was an inventive concept by June 17, 1999, or even June 25, 1999, that was the same as the subject matter of the count. Thus, the testimony in that regard is speculative and unsupported.

Additionally, Dr. Tsern is a co-inventor and cannot provide the independent corroboration that is required. *See Brown v. Barbacid*, 276 F.3d at 1335.

For the reasons discussed above, Perego has also failed to demonstrate conception of the subject matter of the count by June 25, 1999.

I. Conclusion

Junior party Perego has not established priority of invention over senior party Drehmel. It is not necessary to consider senior party's priority motion.

Because Perego has failed to meet its burden in establishing conception of the subject matter of the count by any one of its three alleged dates of conception, May 14, 1999, June 15, 1999, and June 25, 1999, whether Perego has established reasonable diligence from just prior to Drehmel's conception to Perego's filing date is inconsequential.

Because Perego's motion has not established a prima facie case of priority of invention over Drehmel, we need not consider Drehmel's opposition to Perego's priority motion, or Perego's reply.

Drehmel's Miscellaneous Motion 2 to exclude a multitude of Perego exhibits need not be reached, because even without excluding any Perego exhibit Perego's Motion 9 has not established conception of the subject matter of the count on May 14, 1999, June 15, 1999, or June 25, 1999.

J. Order

It is

ORDERED that Perego's Motion 9 is *denied;*

FURTHER ORDERED that Drehmel's Motion 1 is *dismissed*; and

FURTHER ORDERED that Drehmel's Miscellaneous Motion 2 to exclude Perego's evidence is *dismissed* as moot.

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